# HIGH DENSITY MICROWAVE PACKAGING PROGRAM PHASE 1 - TEXAS INSTRUMENTS/MARTIN MARIETTA TEAM

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## ABSTRACT

On the ARPA sponsored High Density Microwave Packaging (HDMP) program, a team composed of Texas Instruments (TI), Martin Marietta, and General Electric (GE) is developing a packaging system to support tile conformal phased arrays. Significant volume and weight reductions are projected relative to today's microwave module technology. The team's approach utilizes a stacked module configuration, with a surface contact vertical interconnect between module layers. The module layers are built on a metal matrix composite AlSiC substrate with silicon and MMIC devices mounted face-up in substrate wells. Chip-to-chip interconnect is provided by an enhanced version of Martin Marietta's Microwave High Density Interconnect (MHDI) process. Stacked module assemblies are surface mounted on an RF/DC manifold on the back of the conformal array surface. Incremental technology demonstrations are planned as part of the program, culminating in a 96-element brassboard array demonstration.

## INTRODUCTION

The purpose of the HDMP program is to provide the technology advancements to implement affordable conformal phased arrays for next generation aircraft and space based radars. The 48-month program, which started in July 1993, is sponsored by the ARPA Electronic Systems Technology Office, managed by the Air Force Wright Laboratory Electronics Directorate, and receives tri-service oversight. The TI, Martin Marietta and GE team is developing an array configuration utilizing a stacked, tile module approach based on an enhanced MHDI technology. This will require significant breakthroughs in module interconnect, housings, interfaces and fabrication techniques. Key features of the packaging system are:

- A multilayer stacked tile module assembly concept
- Surface contact vertical interconnect (module layer to layer and module to manifold)
- Enhanced seven-layer MHDI within the module with buried passive RF structures
- MMICs packaged with a dielectric cap and ground shield to provide for RF isolation
- An RF/DC manifold, also implemented using MHDI
- A one-piece array structural and cooling faceplate
- A low-cost single-piece radiator/circulator assembly
- Thin (<1 inch) overall array.

An extremely important aspect of the program is that the packaging technology must be low cost once it reaches volume production. A cost model has been developed and current projections are that per-channel T/R module costs of less than $300 in high volume production are feasible. Array costs (including T/R modules, faceplate, manifold, radiating elements, and other array-mounted electronics) of approximately $600 per channel are also projected.

This program includes incremental technology demonstrations and will culminate in the final demonstration of a functional, 96-element conformal array brassboard.

## PROGRAM OBJECTIVES

Table 1 describes objectives for the program. Significant reductions in size and volume are projected, both at the module and array level. The module level volume and weight improvements are even more substantial if energy storage capacitors, which are not a target of improvement on the program, are removed from the comparisons.

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**Table 1. Program Performance Objectives**

| | |
|---|---|
| Array Level | |
| Weight Reduction | 2.5:1 |
| Volume Reduction | 5:1 |
| Thickness | <1 inch |
| Module Level | |
| Weight Reduction | 5:1 |
| Volume Reduction | 4:1 |
| Thickness | 0.27 inch |
| Frequency | X-Band |
| Peak power/channel | 10 W |

## PACKAGING APPROACH DESCRIPTION

The array concept for the TI team is shown in Figure 1. For a typical 2,000-element phased-array antenna, a single-piece conformal structural faceplate will provide structural rigidity, mounting for the manifold, modules and radiating elements and liquid cooling channels for the active



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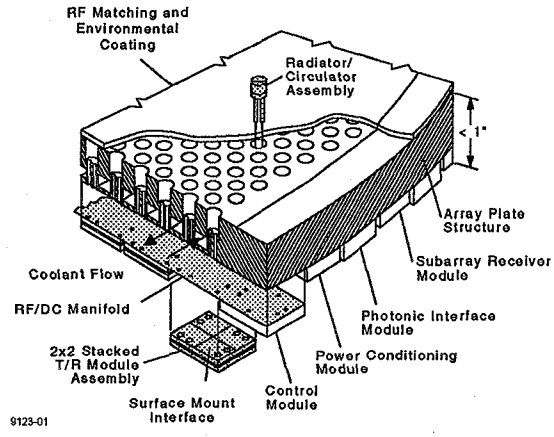


**Figure 1. Proposed Array Concept**

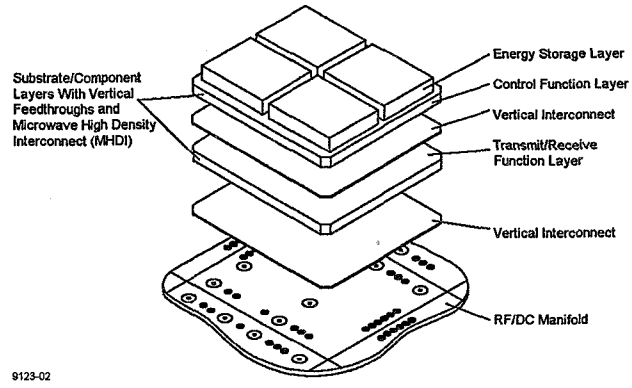


**Figure 2. Stacked Tile Module Assembly**

array. Implementing the faceplate as a single piece will eliminate issues associated with seams between conventional subarray or slat subassemblies, reducing the radar cross section (RCS). The thin array, less than one inch including modules, enables conformal arrays and frees volume for other electronics. Radiator/circulator assemblies are mounted in wells in the faceplate, with RF interfaces provided by coaxial spring pin connections to the RF/DC manifold mounted on the back of the faceplate. A wide-angle impedance matching (WAIM) and environmental coating sheet is bonded to the front of the faceplate. The RF/DC manifold is attached to the back of the faceplate. It provides interconnect for power, control, and RF interfaces, performs beamformer functions, and is implemented using MHDI technology. Modules are surface mounted to the manifold. Most of these would be T/R modules, but around the perimeter of the array other modules would be mounted in a similar manner. These would include power conditioning, control, and subarray driver and receiver modules.

Figure 1 and the above paragraph describe a full array implementation. On the HDMP program, the TI team will implement a subset of this for the brassboard array, populating it with 96 T/R channels and radiator/circulator assemblies, small area RF/DC manifolds, and a reduced size conformal faceplate with matching sheet.

The module physical configuration is shown in Figure 2. It is a vertically stacked configuration, with two active layers and one passive energy storage layer. The layer closest to the faceplate contains the front end transmit and receive components and any high power-dissipation regulation devices. The other active layer contains the remaining receive and transmit amplifier stages, as well as the phase shifter and controller devices. Each active module layer is built on a metal matrix composite AlSiC substrate with silicon and MMIC devices mounted face-up in substrate wells. Each stacked tile module assembly contains four 10-watt-per channel transmit/receive functions, configured in a $2 \times 2$ array. The brassboard array will consist of 24 of these $2 \times 2$ element module assemblies.

MMIC devices will be capped utilizing a dielectric layer with vias through the dielectric to bring MMIC pads to the cap surface. A top surface ground plane will also be incorporated. The purpose of capping is to provide isolation between MMICs and allow for routing of RF and DC signals in the MHDI circuit directly above the MMIC. This new capping process represents one of the most significant challenges on the program and is being addressed early. Achieving a close CTE match between the dielectric cap material and GaAs is critical. Formation of high aspect ratio vias from the MMIC surface pads through the relatively thick (10-mil) cap is challenging. The impact of the overlying dielectric and ground plane on MMIC performance must be characterized, although early prototype efforts showed this to be a minimal impact. Future MMICs would be designed to account for the cap presence and compensate for it. Because MMICs represent such a high percentage of the overall module cost, the impact on fabrication yield must be minimal. Some positive yield benefits are expected to accrue as the cap layer will serve to ruggedize the MMIC both at the wafer and chip level, but the new fabrication steps must not significantly degrade yield.

Chip-to-chip interconnect is provided using an enhanced version of the MHDI process. MHDI is a polymer and metal interconnect system, built over a substrate populated with devices mounted face-up in wells. It is a high-yield, wire-bondless process that provides a very high-density controlled impedance interconnect. Enhancements being implemented to Martin Marietta's baseline process include increasing the number of layers from

three to six, increasing the thickness of some of the polymer layers, implementation of passive functions such as couplers and buried resistors in the interconnect circuit, and the addition of a metal and inorganic hermetic barrier over the top of the circuit.

The substrate for each layer is a metal matrix composite (MMC) AlSiC casting with pockets for components and with vertical feedthroughs for RF, DC, and control signals. The substrate is 50 mils thick and does not contain tall thin walls, like most RF module housings built today. The overall substrate must be hermetic so that after the MHDI circuit is fabricated with its hermetic top layer, an overall hermetic subassembly is achieved. A key objective of the program is affordability, and this is reflected in the fabrication objectives for the substrate. The feedthroughs are being captured in situ as part of the MMC infiltration process. Near-net-shape fabrication must be achieved, including the precision depth of the chip wells. Process yields must be very high, approaching six-sigma levels, to meet the future cost objectives. Statistical measurements and design of experiment techniques are being used as part of the development to assure that these goals are reached. Plating of ceramic substrates has traditionally been a problem and is receiving special attention.

Electrical and thermal interconnect between layers will be provided by an elastomeric z-axis vertical interconnect circuit. This interface is particularly challenging as it must be thin for maximum thermal and electrical conductivity and yet must conform to the module layer surfaces. The circuit is manufactured utilizing Elastomeric Conducting Polymer Interconnect (ECPI) a material developed and supplied by AT&T. To provide sufficient compliance to the surfaces the basic material is modified by adding a pattern of holes in the interface circuit. While reducing the conductivity somewhat, the holes allow material in the thin film to deform laterally as the film is compressed and conforms to the uneven surface.

Stacked module assemblies are surface mounted to the array manifold on the back of the conformal array surface utilizing the same elastomeric vertical interconnect material as is used between the module layers. The entire assembly is attached to the back of the array using screw clamping hardware. This aligns each module assembly to the array manifold and provides the correct compression force on the elastomeric interconnect material. Maintenance is also easily accomplished using this attachment and interface method.

## ACCOMPLISHMENTS AND FUTURE PLANS

In the first 18 months of the program, the TI, Martin Marietta and GE team has concentrated on the most challenging technology enhancements needed to implement the tile modules. Array level issues will be addressed later in the program.

A significant portion of the program has focused on dielectric material development and development and integration of all of the necessary processes for MMIC capping at the wafer level. Dielectric cap material has been fabricated with a CTE of 7 ppm/°C, a very close match to that of GaAs. The material is fabricated by Cast Metal Composites (CMC) of Cleveland, Ohio, as a cyanate-ester/quartz polymer matrix composite. In November 1994, the first fully capped MMIC test structures were successfully fabricated at Texas Instruments with a via level yield of approximately 91 percent. Capped structures are shown in Figure 3. The first capped active devices will be completed in the first quarter of 1995. Demonstration of the overall process on active devices, improvement of capping yield, reduction of capping costs, characterization of performance impact on the MMIC and completion of the active devices needed to build the brassboard array are future tasks.

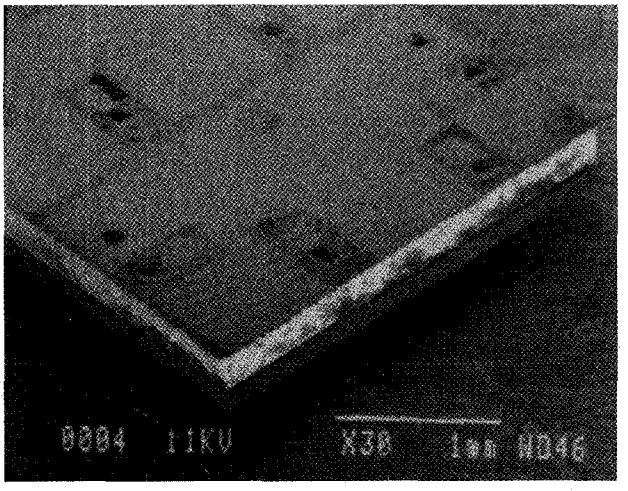


**Figure 3. Early Capped MMIC Test Structures**

Metal matrix composite AlSiC substrates were successfully near-net-shape fabricated by Ceramics Process Systems (CPS) of Chartley, Massachusetts, with feedthroughs captured as part of the infiltration process. The substrate is shown in Figure 4. Plating quality and yield levels improved substantially through several part lots and met the objectives of this phase of the program. Dimensional accuracy of the substrates were achieved including the critical chip well depth dimensions. Feedthrough hermeticity was not achieved in this first phase because of some cracking of the RF feedthroughs. Correction of this problem and improvement of the plating process yield are tasks planned for the next program phase.

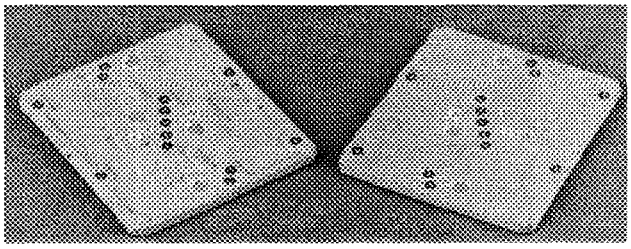

**Figure 4. Metal Matrix Composite Substrate**

MHDI baseline process enhancements, which were demonstrated at GE CRD, included fabrication of six-layer circuits with buried passive components, and thicker polymer layers. Standard evaluation circuits (SECs) were fabricated and met all their yield and performance expectations. The via strings in the MHDI circuit achieved 100-percent yield on over 60,000 vias. In the next phase of the program, some circuit adhesion yield issues must be addressed and the metal hermetic barrier process will be demonstrated.

GE CRD also developed and demonstrated a process to fabricate the free-standing MHDI manifold circuits. This process was used to fabricate three-layer manifolds for an early integrated demo planned for later in 1995, shown in Figure 5. In the next program phase, larger area manifold circuits containing up to six layers will be fabricated and demonstrated.

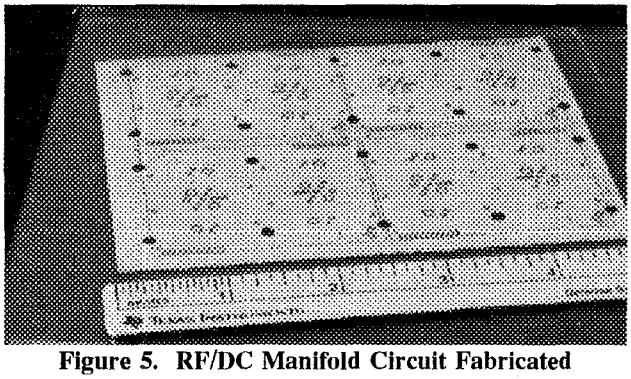

**Figure 5. RF/DC Manifold Circuit Fabricated with MHDI Process (Four Circuits Shown)**

Vertical interconnect circuits were fabricated with the softening features to allow for compression to achieve electrical conductivity. Electrical DC and RF conductivity measurements were made using a substrate, interconnect circuit, and the manifold circuits manufactured by GE. These electrical and RF measurements met specifications, although thermal performance has been below requirements. Reaching the desired thermal conductivity is a goal of the next phase of the program and is expected to require some modification of the basic ECPI material.

Preliminary module layouts have been completed by Martin Marietta Laboratory • Syracuse for each of the two active layers, and an initial demonstration configuration has been designed in detail for the transmit layer. The manufacturing and engineering groups at Martin Marietta Government Electronic Systems (GES) participated on the integrated product/process team for design consultation and concurrent engineering. This module layer will be built as part of an Initial Technology Demonstration (ITD) later in 1995. The ITD will combine a module layer, built using the AlSiC substrate, capped MMIC test structures and active devices, interconnected using the six-layer enhanced MHDI process, and with the elastomeric z-axis vertical interconnect circuit, mounted on an MHDI manifold in an integrated assembly. This will allow evaluation of overall interconnect and module performance early in the program and will identify process and design enhancements needed prior to building the brassboard. Following RF evaluation, this ITD configuration will be subjected to testing to identify any reliability issues that need to be addressed. Later in the program, final designs for the transmit/receive and control layers will be completed and used in the 96-element brassboard array. The modules for the brassboard will be built on the Martin Marietta GES MHDI production line in Moorestown, New Jersey.

Initial radiating element and array configurations have been defined, although detailed design is planned for the later phases of the program.

## CONCLUSION

The HDMP packaging configuration, when fully developed, will represent a major advancement in packaging density and performance for conformal tile phased arrays at an affordable cost. The packaging approach will be applicable to a very broad range of planar and conformal applications in both brick and tile configurations. Although insertion in conformal tile array system applications is still several years away, the advancements in the constituent technologies including MMIC capping, vertical interconnect, metal matrix composite substrates and enhanced MHDI are expected to have nearer term, spin-off applications. In the first 18 months of the program, significant progress has been made on the critical technology enhancements for the program. Continued progress at this same pace will lead to successful demonstration of all of the program objectives.